

1. (Currently Amended) A video signal processing system for processing a video data V_{IN} and graphic data $D_{\mu P}$, comprising:

a) a filter unit, which receives the video data V_{IN} , and horizontally and vertically filters the video data V_{IN} to convert the video data V_{IN} into video pictures formatted with a different number of columns and/or lines, and provides a filtered video signal indicative thereof, wherein thesaid filter unit buffers individual pixels and/or lines in a first memory device;

b) a second memory device that receives and stores the graphic data $D_{\mu P}$ and thesaid filtered video signal and provides stored signals indicative thereof;

c) a third memory device that is connected to thesaid second memory, and stores data received from thesaid second memory devices; and

d) a mixing unit that receives and mixes thesaid stored graphic data and thesaid stored filtered video data to provide a video output signal V_{OUT} .

2. (Currently Amended) The video signal processing system of claim 1, wherein thesaid first memory device comprises random access memory.

3. (Currently Amended) The video signal processing system of claim 1, wherein thesaid second memory is configured as fast cache memory.

4. (Currently Amended) The video signal processing system of claim 13, wherein thesaid third memory device comprises random access memory.

5. (Currently Amended) The video signal processing system of claim 12, wherein thesaid graphic data ~~$D_{\mu P}$~~ comprises bitmaps received from a ~~micro~~processor.

6. (Currently Amended) The video signal processing system of claim 12, comprising:
a controller that controls thesaid filter unit, thesaid first, second and third memories and thesaid mixing unit to control the processing of thesaid video signal processing system.

7. (Currently Amended) The video signal processing system of claim 6, wherein thesaid video signal processing system operates in real time with the clock frequency of thesaid controller being higher than the clock frequency of the signal associated with the video data V_{IN} and thesaid video output signal V_{OUT} .

8. (Currently Amended) The video signal processing system of claim 6, wherein the said controller comprises a ~~micro~~processor.

9. (Currently Amended) A video signal processing system for processing a video data V_{IN} and graphic data ~~$D_{\mu P}$~~ , comprising:

a) a horizontal filter that receives and converts the video data ~~V_{IN} and converts the video data V_{IN}~~ into video pictures formatted with a different number of columns, and provides a horizontally filtered video signal indicative thereof, wherein thesaid horizontal filter buffers individual pixels and/or lines in a first memory ~~device~~;

b) a second memory-device that receives and stores the graphic data $D_{\mu P}$ and thesaid horizontally filtered video signal and provides stored signals indicative thereof;

c) a third memory-device that is connected to thesaid second memory, and stores data received from thesaid second memory-devices; and

d) a mixing and filtering unit that receives thesaid stored graphic data and thesaid stored horizontally filtered video data, vertically filters thesaid stored horizontally filtered video data to convert the video data into video pictures with a different number of lines and provide a vertically filtered signal indicative thereof, and mixes thesaid stored graphic data with thesaid vertically filtered video signal to provide a video output signal V_{OUT} .

10. (Currently Amended) The video signal processing system of claim 9, wherein thesaid second memory device is configured as a fast cache memory.

11. (Currently Amended) The video signal processing system of claim 9, wherein thesaid third memory-device comprises random access memory.

12. (Currently Amended) The video signal processing system of claim 9, wherein the graphic data comprises bitmaps received from a microprocessor.

13. (Currently Amended) The video signal processing system of claim 9, comprising:
a controller that controls thesaid horizontal filter, thesaid first, second and third memories and thesaid mixing unit to control the processing of ~~said~~ the video signal processing system.

14. (Currently Amended) The video signal processing system of claim 13, wherein the clock frequency of ~~thesaid~~ controller is higher than the clock frequency of a signal at the video input signal- V_{IN} and ~~thesaid~~ video output signal- V_{OUT} .

15. (Currently Amended) The video signal processing system of claim 14, wherein ~~thesaid~~ controller comprises a ~~micro~~processor.

16. (Currently Amended) The video signal processing system of claim 945, wherein ~~thesaid~~ video signal processing system is used for interlace progressive conversion.

17. (Currently Amended) A video signal processing system for processing a video data- V_{IN} and graphic data- $D_{\mu P}$, comprising:

a filter unit, which receives the video data- V_{IN} and ~~horizontally and vertically~~ filters the video data- V_{IN} to convert the video data- V_{IN} into video pictures formatted with a different number of columns and/or lines, and provides a filtered video signal indicative thereof, wherein ~~thesaid~~ filter unit buffers individual pixels and/or lines in a first memory-~~device~~;

b) a second memory-~~device~~ that receives and stores the graphic data- $D_{\mu P}$ and ~~thesaid~~ filtered video signal and provides stored signals indicative thereof;

c) a third memory-~~device~~ that is connected to ~~thesaid~~ second memory, and stores data received from ~~thesaid~~ second memory devices; and

d) a mixing unit that receives and mixes thesaid stored graphic data and thesaid stored filtered video data to provide a video output signal V_{OUT} , ~~which represents a superposition of said stored graphic data and said stored filtered video data.~~

18. (Currently Amended) A video signal processing system for processing a video data V_{IN} and graphic data $D_{\mu P}$, comprising:

a) a horizontal filter that receives and converts ~~the video data~~ V_{IN} ~~and converts~~ the video data V_{IN} into video pictures formatted with a different number of columns, and provides a horizontally filtered video signal indicative thereof, wherein thesaid horizontal filter buffers individual pixels and/or lines in a first memory ~~device~~;

b) a second memory ~~device~~ that receives and stores the graphic data $D_{\mu P}$ and thesaid filtered video signal and provides stored signals indicative thereof;

c) a third memory ~~device~~ that is connected to thesaid second memory, and stores data received from thesaid second memory ~~devices~~; and

d) a mixing and filtering unit that receives thesaid stored graphic data and thesaid stored horizontally filtered video data, vertically filters thesaid stored horizontally filtered video data to convert the video data into video pictures with a different number of lines and provide a vertically filtered signal indicative thereof, and mixes thesaid stored graphic data with thesaid vertically filtered video signal to provide a video output signal V_{OUT} .